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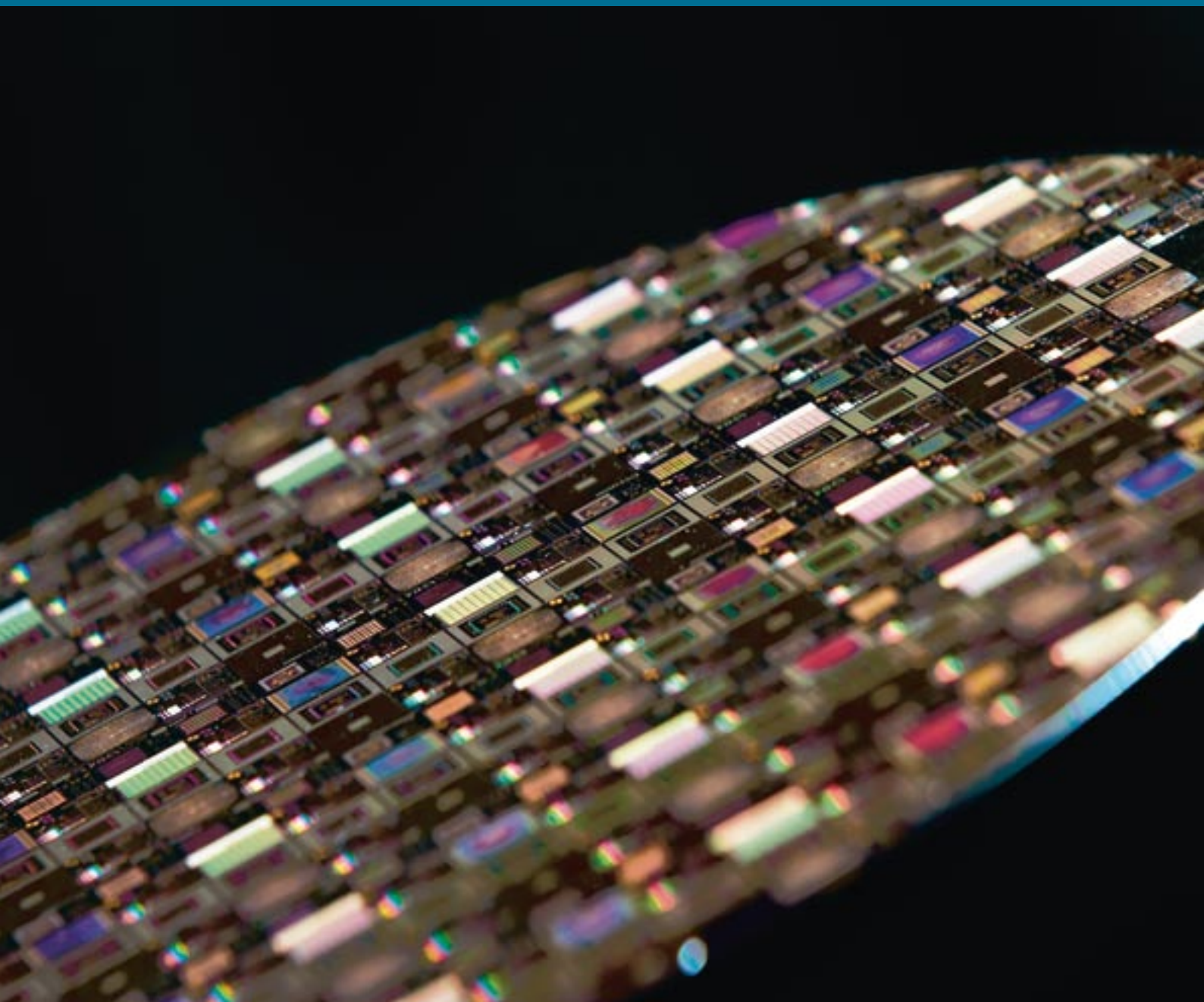
ALL SILICON SYSTEM INTEGRATION DRESDEN



ALL SILICON SYSTEM INTEGRATION DRESDEN FRAUNHOFER IZM-ASSID

FRAUNHOFER IZM

The Fraunhofer Institute for Reliability and Microintegration (IZM) is one of the 12 institutes of the Fraunhofer Group for Microelectronics. The Fraunhofer-Gesellschaft is one of the leading organizations of applied research in Europe undertaking contract research on behalf of industry. Fraunhofer IZM is a worldwide renowned institute specializing in developing advanced packaging and system integration technologies and transferring research results to the industry and thus being able to offer customer-specific solutions for microelectronic products in the overall scope of smart system integration.

LEADING EDGE MICRO-ELECTRONIC PACKAGING AND SYSTEM INTEGRATION

WL-SIP PROTOTYPING PILOT LINE

FRAUNHOFER IZM-ASSID

The center "All Silicon System Integration Dresden – ASSID" operates Fraunhofer IZMs leading edge, industry-compatible 200/300 mm 3D wafer-level process line with modules for TSV formation, TSV post-processing, pre-assembly, wafer-level assembly, stack formation and with related metrology tools. ASSID is focusing on process development, material and equipment evaluation as well as R&D services. It is a partner in national, European and worldwide industrial and scientific networks for 3D system integration, e. g., ITRS, ENIAC, Catrene, EPOSS, Euripides, SEMATECH and Silicon Saxony. Fraunhofer IZM-ASSID has established cooperation and joint development programs with industrial partners for undertaking material and equipment evaluation, process development as well as process and product integration.

FRAUNHOFER IZM-ASSID TARGETS

- Fraunhofer IZM-ASSIDs vision is the heterogeneous integration of multi-functional electronic devices into one wafer-level system-in-package (WL-SiP) by using enhanced 3D integration, interconnection and assembly technologies.
- Fraunhofer IZM-ASSID develops leading-edge technologies for 3D system integration on 200/300 mm wafers and provides customized technology development, process transfer and product integration.
- Fraunhofer IZM-ASSID offers material, process and equipment evaluations and qualification for industrial partners.
- Fraunhofer IZM-ASSIDs services include customer-specific prototyping as well as pilot line manufacturing.

HETERO-GENEOUS WAFER-LEVEL SYSTEM INTEGRATION

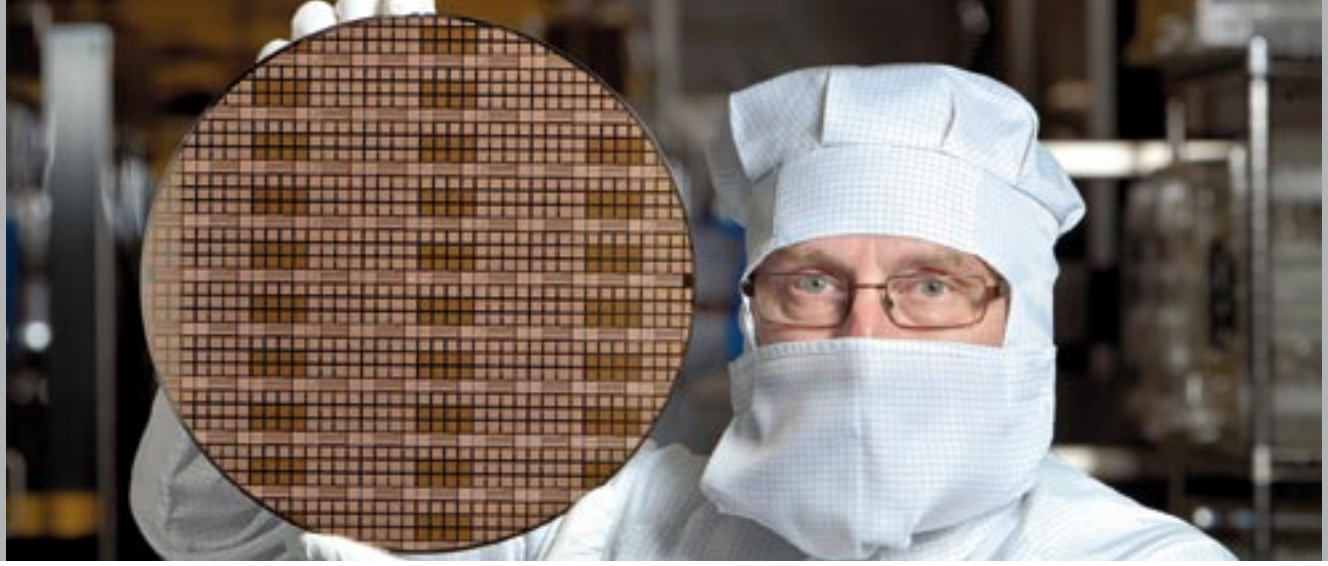
COVERING ALL ASPECTS OF 3D INTEGRATION

FRAUNHOFER CLUSTER 3D-INTEGRATION

With its outstanding competencies in the fields of technology, design, analytics and reliability, the Fraunhofer-Gesellschaft offers excellent prerequisites for the market-oriented implementation of 3D smart systems. To cope with the complexity of this technological approach, leading Fraunhofer institutes (IZM-ASSID, ENAS, IZFP, IIS/EAS, IPMS) cluster their competencies in a network which is in this way able to cover a broad spectrum of topics related to 3D integration.

www.3D-integration.fraunhofer.de

Cover picture: 300 mm Cu-TSV interposer with integrated passive devices (G2)

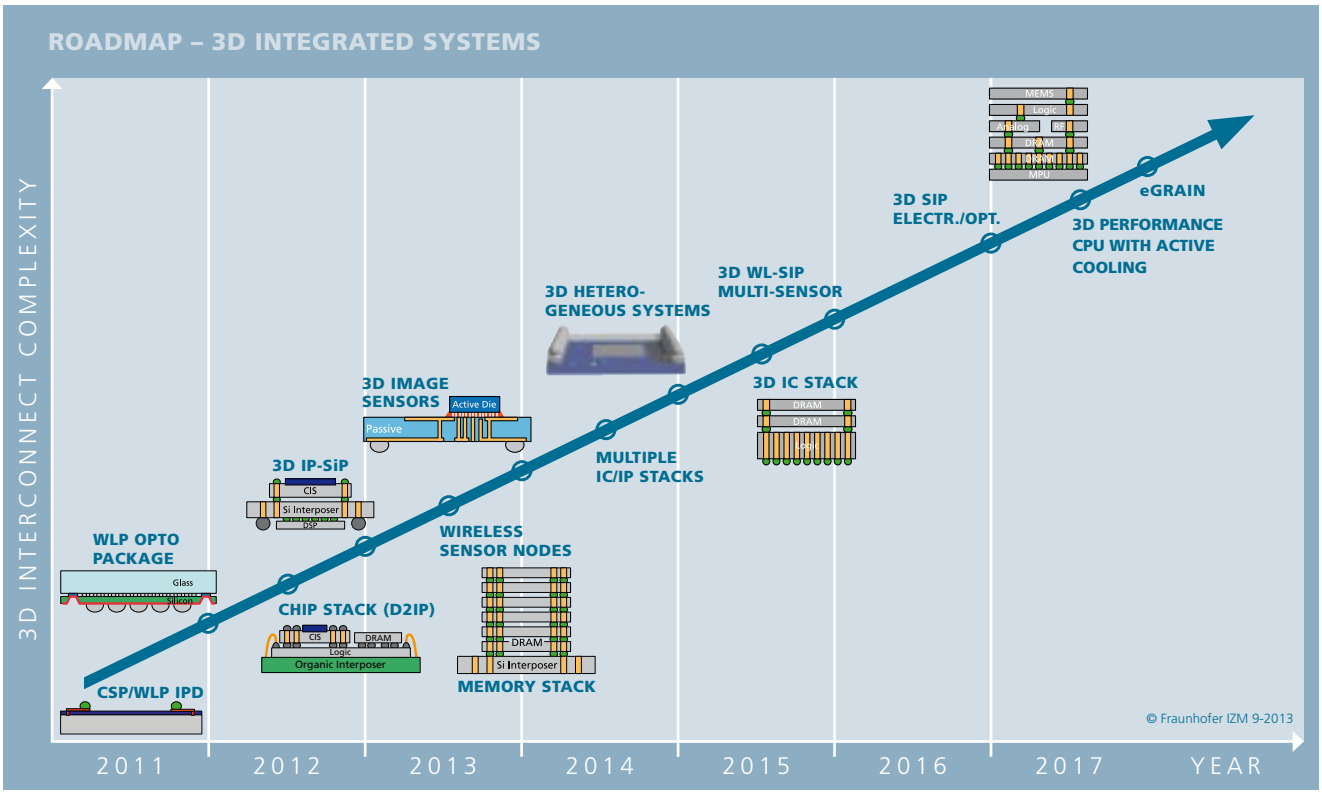


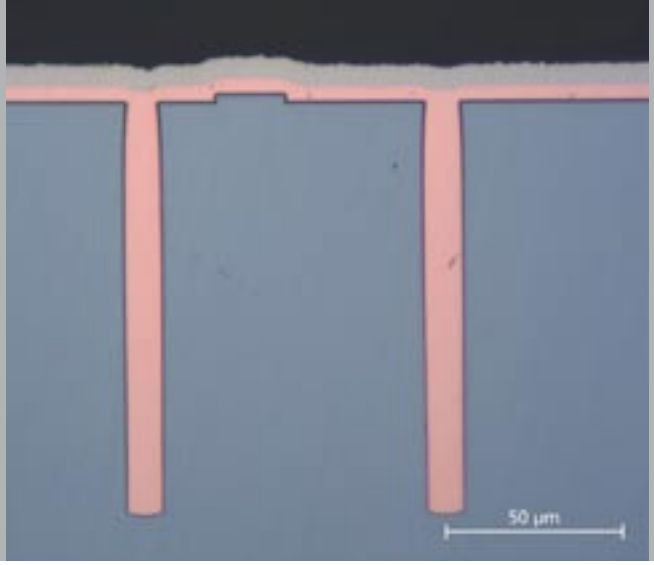
HETEROGENEOUS 3D WAFER-LEVEL SYSTEM INTEGRATION

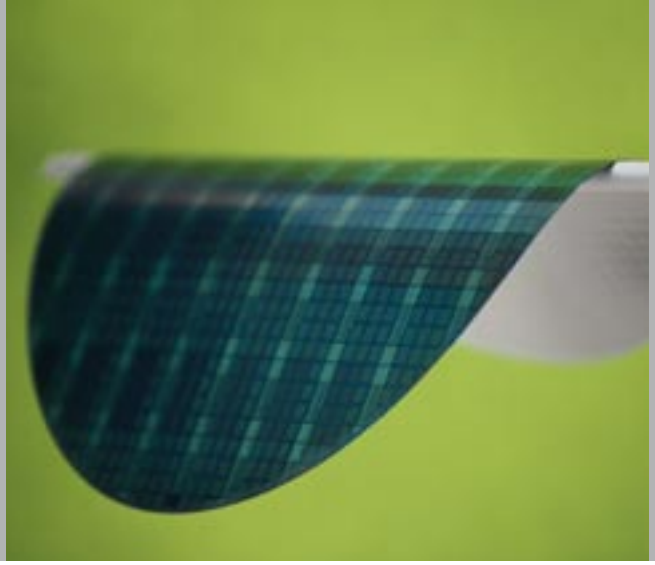
3D integration is of high significance for the realization of future innovative products and a key enabler to deal with the technical requirements e.g., performance, form factor and functionality for smart systems in different application fields like information & communication, security, healthcare, mobility & transportation and industrial electronics. It allows the multi-device integration of sensors, processors, memories and transceivers into one optimized wafer-level system-in-package (WL-SiP). Therefore, scientific and industrial research is focusing on developing 3D integration technologies to enable 3D smart systems.

Main technology tasks:

- 3D wafer-level system integration (wafer size: 200/300 mm)
- Through silicon via formation (Cu-TSV)
- Silicon interposer with multi-layer high-density redistribution
- Wafer thinning and thin wafer handling
- Temporary wafer bonding and de-bonding
- Wafer bumping (ECD and solder preform)
- Die-to-wafer and wafer-to-wafer bonding
- Wafer-level assembly and 3D stacking







THROUGH SILICON VIA (TSV) FORMATION

Through silicon vias (TSV) are a key element in 3D wafer-level system integration. Fraunhofer IZM-ASSID has developed a TSV process for customer-defined applications based on Cu-ECD filling. All processes are carried out using leading-edge, industry-compatible process equipment for 200/300 mm wafers.

Main technology tasks:

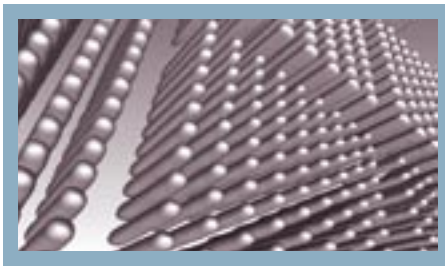
- High-density Cu-TSV technology for advanced system performance: TSV diameter: typ. 5–20 µm; aspect ratio: 5–12
- Cu-TSV filling using high-speed ECD
- Application-specific dimensions diameter/depth:
  - min. 5 µm/50 µm
  - typ. 10 µm/120 µm
  - 20 µm/120µm
  - backside TSV (Cu-liner) up to 250–700 µm depth
- Via middle & via last approach and backside via last formation for active circuit devices
- Evaluation and qualification of new materials for isolation, barrier/seed and TSV filling
- Optimized TSV post-processing (frontside and backside)

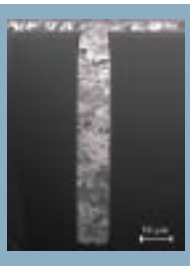
WAFER THINNING, AND THIN WAFER HANDLING

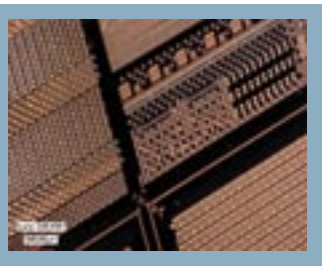
Wafer thinning and thin wafer handling technologies are an integral part of the TSV process integration as well as essential for the realization of 3D system architectures. Continuous optimization of these technologies is indispensable to meet the requirements of cost-effective manufacturing and the realization of 3D systems.

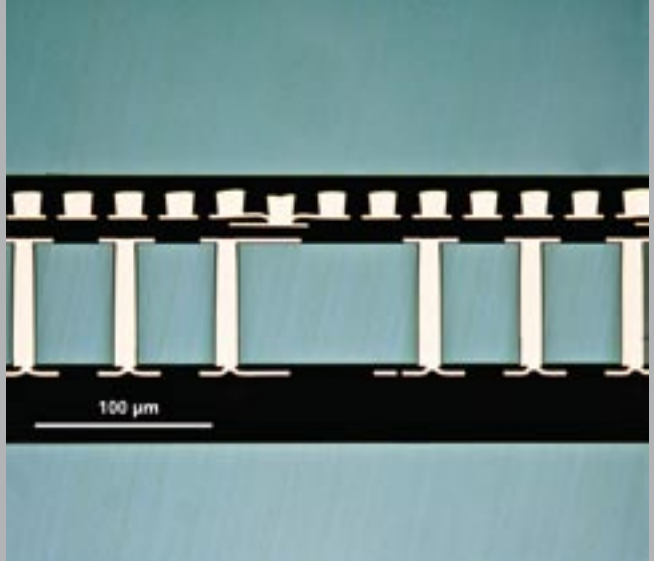
Main technology tasks:

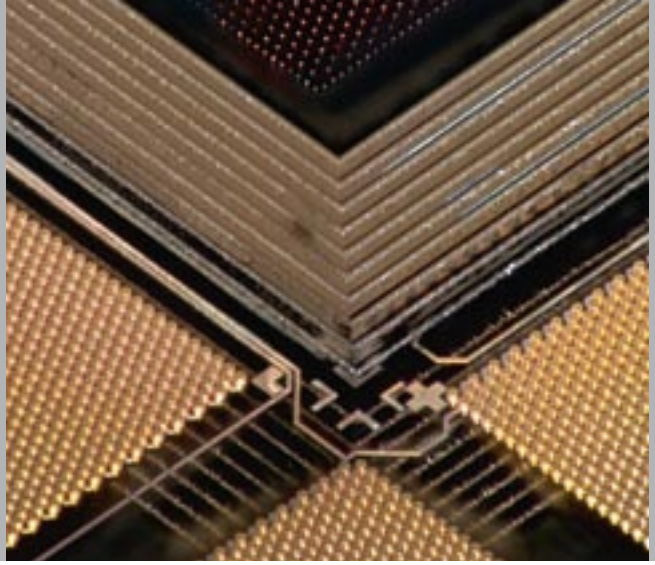
- Optimization of temporary wafer-bonding and de-bonding technologies (device wafer thickness: > 20 µm; multiple repeatable bonding and de-bonding processes)
- Enhanced wafer thinning and stress relief technologies for ultra-thin wafers (> 20 µm)
- Enhanced dicing technologies using low k-materials, small dicing streets (< 40 µm) and reduced mechanical edge and corner damage to wafer frontside and backside











TSV-INTERPOSER WITH HIGH-DENSITY REDISTRIBUTION

The TSV interposer is used as a carrier to meet the technical specifications of integrated circuits e.g., geometry, high number of I/O and their high-density routing. According to the application, multi-layer high-density wiring on frontside/backside down to < 2 µm line/space as well as Cu-TSVs with diameters between 5–20 µm are required. The functionality of Si-interposers will be extended by the integration of passive devices such as inductors, resistors and capacitors - with an emphasis on RF applications. Next generations will also include integrated active devices and deal with high power dissipation by applying innovative cooling architectures and will also address the integration of electrical/optical interconnects for high speed data transmission. These new generations of Si-interposers are the basic prerequisite for modularized 3D stacked architectures for fully heterogeneous system integration.

Main technology tasks:

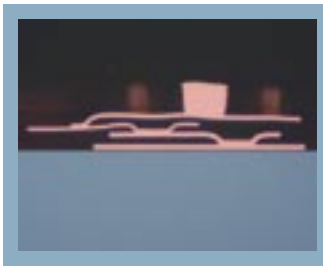
- Interposers with high-density Cu-TSV
- High-density multi-layer copper wiring: > 2 µm line/space, 4-layer frontside RDL, up to 3-layer backside RDL
- Integration of passive devices (R, L, C)
- Embedding of active and passive devices
- Interconnects for 3D stacking of devices/substrates
- Thermal management

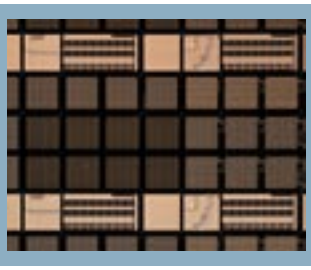
ASSEMBLY AND INTERCONNECTION TECHNOLOGIES

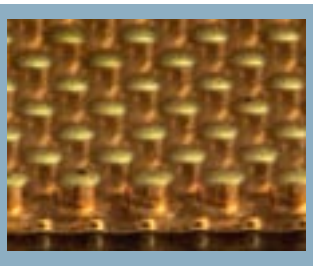
Assembly and interconnection technologies relevant for 3D system integration are strongly affected by IC technology nodes. Key parameters include die size, number of I/O, pad geometries, passivation layers, wafer-surface topologies, terminal pads and limitations to the thermal budgets that can be applied during assembly. Additional challenges in assembly and interconnect technologies for 3D systems include alignment accuracy, yield requirements and productivity that meet the demands of cost effective manufacturing.

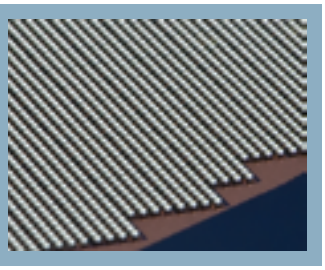
Main technology tasks:

- Evaluation of die-to-wafer (D2W), die-to-interposer (D2IP) and wafer-to-wafer (W2W) assembly technologies
- 3D IC assembly with high-density interconnects (> 1000 I/O) and ultra-fine pitch (> 50 µm)
- IC assembly with thin and ultra-thin chips (20–150 µm)
- Evaluation of low-temperature assembly technologies
- Evaluation of flux-free solder connections with self-alignment capability
- 3D stack formation









SERVICES

Fraunhofer IZM-ASSID provides prototyping services and its facility with leading-edge, industry-compatible equipment is open to companies for research and development activities as well as material, equipment & process evaluation and improvement.

Technological services include:

- TSV silicon interposer
- 3D TSV via middle/via last process integration
- Deposition and patterning of dielectric polymers and metal films
- Multi-layer Cu redistribution with customer-specific terminal pad metallurgies (Cu, Cu/Ni/Au, Cu/SnAg)
- Wafer thinning and thin wafer processing
- Wafer-level bumping (Cu-Pillar, SnAg, CuNiAu)
- Wafer-level solder ball attach (100–500 µm)
- Wafer-level assembly
- Die attach (lamination, epoxy, flip chip) on various substrates
- Component assembly (bare die, active and passive SMD components)
- Customer-specific prototyping and pilot line manufacturing
- Material and equipment evaluation, process development, process transfer and product integration

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