Fraunhofer IZM

High-End Performance Packaging

Hermetic Wafer-Level MEMS Packaging

Fast Facts

1. Depending on the wafer and component size, up to several 10k MEMS devices can be hermetically packaged in parallel at one wafer.
2. Technology was demonstrated for real-time clock functionalities with one LF and two HF fully programmable output frequencies.
3. Example of a SiP with the smallest dimensions of 1.64 x 1.25 x 0.65 mm³

The connection of active or passive TSV silicon interposer wafers with cap wafers by wafer-to-wafer bonding technologies offers new possibilities for hermetic wafer level packaging of MEMS components.

Based on its 200 mm/300 mm-compatible advanced wafer-level packaging process lines, Fraunhofer IZM can support new hermetic wafer-level MEMS packaging concepts. The process scheme includes TSV formation into a passive interposer or active CMOS wafers including wafer thinning and thin wafer processing on temporary carrier wafers for TSV back side reveal and RDL/contact formation on the back side of the wafer.

The MEMS are then assembled onto the back side of the thin TSV wafer which is done by sequential or collective die-to-wafer bonding. Additionally, cap wafers are manufactured with recesses and metal-bonded frames to fit the corresponding TSV wafers with the mounted MEMS exactly. Finally, the cap wafers are bonded to the TSV wafers using a dedicated soldering regime. This allows all mounted components to be hermetically sealed in an inert atmosphere or vacuum.

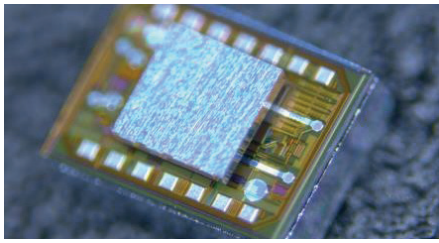
The approach was evaluated for wafer-level packaging of generic timing microsystems incl.:

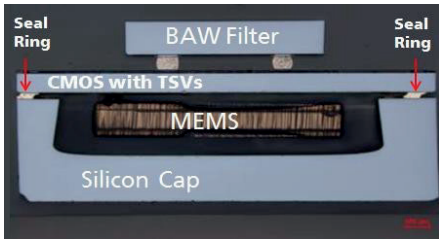
- specially designed timing ASIC built in TSMC CMOS technology
- a miniature quartz tuning fork with 131 kHz resonance frequency
- a 2-GHz bulk acoustic wave (BAW) filter device

The ASIC wafers were processed with 100 µm deep Cu TSVs on the front side via the last regime. During the backside processing of the ASIC wafers, proper gold structures were created for the assembly of the quartz components and gold/tin frame structures for the bonding of the cap wafers.

The fabricated cap wafers had a thickness of 400 µm. On these wafers, gold metal frames were created which in pitch and lateral dimensions match the frames of the AISC. Inside these frames, 200 µm deep recesses were etched to generate space for the quartz crystals.

Both ASIC and cap wafers were bonded together in a vacuum with standard wafer bonding equipment using a gold/tin soldering regime. After the wafer bonding step, the BAW filter devices were mounted on the front side of the ASIC wafer using reflow soldering.





Top and cross-sectional views of a wafer-level packaged timing microsystem based on TSV CMOS IC bonded with silicon cap, hermetically sealed quartz crystal, and the top side of a mounted BAW filter.

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