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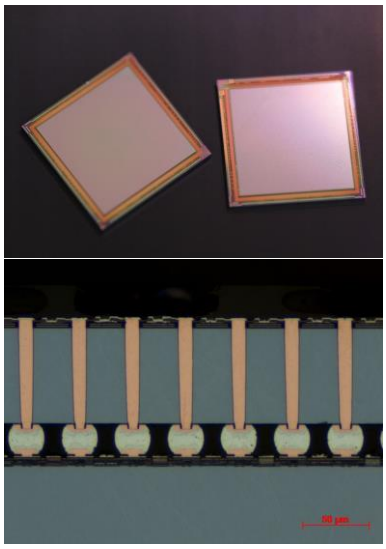
LIDAR Sensor 3D-SiP using High Density TSV Technology



88 µm thin chip with 256x256 SPAD array and TSVs mounted on ASIC in macroscopic and cross sectional view

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Through silicon via (TSV) technologies enable 3D packaging concepts for various types of sensor systems. Fraunhofer IZM offers custom specific process development, prototyp fabrication and small scale production for the post BEOL integration of TSVs into active IC wafers as well as required redistribution (RDL), metallization and assembly processes.
The services include in detail the implementation of DRIE processes to etch blind holes with straight side walls through the BEOL and further down into the bulk silicon of the IC wafers. The holes are isolated by CVD and metallized by PVD for barrier and seed layer deposition followed by complete copper filling using electro-chemical deposition. Interconnections between TSVs and original chip IOs are formed by typical thin film RDL processes. The TSV blind plugs are later accessed from the back side of the wafers by silicon thinning, depositioning and opening of isolation layers as well as deposition of RDL structures or contact pads. Typical TSVs have diameters in the range of 5-20 µm and aspect rations between 5 and 12. Post BEOL TSV integration, which is also known as via last integration, requires metall free zones inside the chips were the TSVs are formed. As part of the service Fraunhofer IZM offers a consultation for chip designer for the proper implementation of these so called keep out zones.

The example images show a macroscopic and cross sectional view of a fabricated LIDAR sensor System-in-Package (SiP) using the described TSV technology.
The system consists of a single photon avalance diode (SPAD) array with 256x256=65536 pixles which is implemented on a 10x10 mm^2 silicon die. The pixles have a pitch of 40 µm. Each SPAD cell includes a TSV which routes the electrical contact to the back side of the SPAD array. The TSVs have a diameter of 8 µm and a depth of 88 µm resulting in a aspect ration of 11. Each of the 65536 TSVs is connected to a micro solder bump with a diameter of 25 µm. The only 88 µm thick SPAD die is connected by these solder bumps to the read out ASIC which has a co-designed read out cell pitch of also 40 µm. The ASIC itself has a size of 12x12 mm^2 with a thickness of 725 µm and was prepared with a copper under bump metallization suitable for the joining of the solder bumps using a pick&place + reflow process.
The read out ASIC has periperal IOs along all four sides for connection by wire bonding. For the next level assembly stage the chip on chip SiP is die bonded to a PCB and ball wedge wire bonded. All packaging related tasks such TSV formation, RDL formation, micro solder bumping as well as flip chip assembly was performed at Fraunhofer IZM in Berlin.