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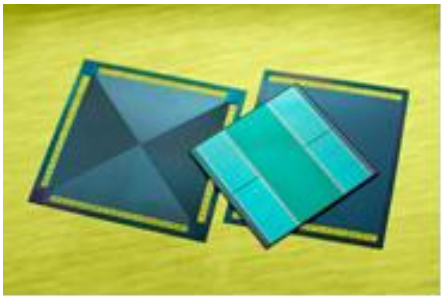

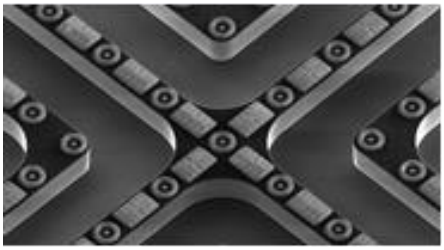

TEST CHIP DESIGN IZM-ASSID MULTI-PROJECT WAFER TC3

Within the European project CarrICool, processes and technologies for the robust manufacturing of modular and scalable interposers using the smart implementation of sophisticated More-than-Moore components are being developed. The new techniques are advancing the System-on-Chip (SoC) and System-in-Package (SiP) evolution and are crucial to improving 3D and beyond-CMOS device integration density. The modular concept combines various microelectronic approaches e.g. interposer technologies, silicon photonics, CMOS technologies, power supply/inductors as well as thermal loss management with respect to integrated water-based cooling concepts. The project with nine european partners is funded by the EU with approx. four million euros and will end in June 2017.

T he maximum processor performance is limited by the heat removal efficiency. Therefore, a highly effective cooling technology as well as an innovative power management are the keys to increase the computing power. Whil air cooling is limited, a liquid cooling approach can meet these high requirements by targeting at a double-sided processor cooling. Within the project CarrICool, IZM-ASSID worked on the realization of a double-sided liquid cooling technology by innovatively integrating horizontal and vertical microfluidic channels.

These micro channels are integrated in an electrically full functional interposer stack with Cu-TSVs in a waterproof manner. With this, for the first time, high performance processors can be additionally and effectively cooled from the bottom side, too. In combination with the integrated cooling plate on the top side of the processor, this double-sided cooling configuration allows the dissipation of 672 W heat from a 4 cm² sized processor surface with a maximum coolant temperature increase of only 60 °C. Compared to the performance of a common kitchen hotplate, this equals a forty times higher heating power when considering the same area size.

Another important aspect for high performance processors is the realization of a high I/O signal bandwidth. Within the project CarrICool, an efficient coupling of optical fibres has been developed. This is based on the integration of structures and solder bumps which enable the self-alignment of the fibres as well as of the chips to the waveguides with a low optical attenuation

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